Disabling the Internal Oscillator on the TMS320VC5507/5509/5509A DSP

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ABSTRACT

This application report contains information and examples on how to disable the internal clock oscillator on the TMS320VC5507, TMS320VC5509, and TMS320VC5509A to minimize power consumption. The document contains an overview of how the internal clock oscillator operates, and how to disable it as part of the IDLE power-down feature. It also discusses how to wake up the oscillator from an IDLE power down.

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1 Overview of IDLE Operations

A critical component of power conservation is minimizing the power used when an application is in an idle or low-activity state. The TMS320VC5507, TMS320VC5509, and TMS320VC5509A incorporate low-activity power management through the implementation of user-controllable IDLE domains. These domains are sections of the device that can be selectively enabled or disabled under software control. When disabled, a domain enters a very low-power idle state in which memory contents are still maintained. When the domain is enabled, it returns to normal operations. The various domains include the central processing unit (CPU), direct memory access (DMA), peripherals, external memory interface (EMIF), and the clock-generation circuitry. For maximum power conservation, the IDLE power-down feature is most commonly used. This feature stops the CPU, DMA, and EMIF domains, except for the internal oscillator with external crystal resonator that is connected to pins X1 and X2/CLKIN. This is shown in Figure 1.

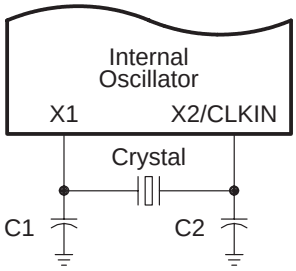

Figure 1. Internal System Oscillator External Crystal

There is a distinction between clock-generation circuitry and the internal oscillator. The clock-generation circuitry refers to the phase-lock loops (PLLs) that are within TMS320VC5507, TMS320VC5509, and TMS320VC5509A. The phase−lock loops provide clock signals to the various internal peripherals and digital signal processor (DSP) core.

The internal oscillator is the input clock source to the clock-generation PLLs. The internal oscillator is not the crystal resonator, but is the circuitry inside the TMS320VC5507, TMS320VC5509, and TMS320VC5509A that drives the crystal to oscillate. By turning off the oscillator, you can further reduce the amount of current consumed. This document outlines, step by step, how to turn OFF the internal oscillator using software as part of the IDLE power-down feature.

The TMS320VC5507, TMS320VC5509, and TMS320VC5509A include two independent clock generators that are sourced by the internal oscillator: the DSP clock generator and the universal serial bus (USB) clock generator. Both clock generators are similar in operation and functionality. The DSP clock generator supplies the clock that is used by the CPU, and all of the other peripherals inside the DSP. The USB clock generator supplies the clock needed to operate the USB peripheral.

The TMS320VC5509 USB clock generator consists of a digital phase lock loop (DPLL) as shown in Figure 2.

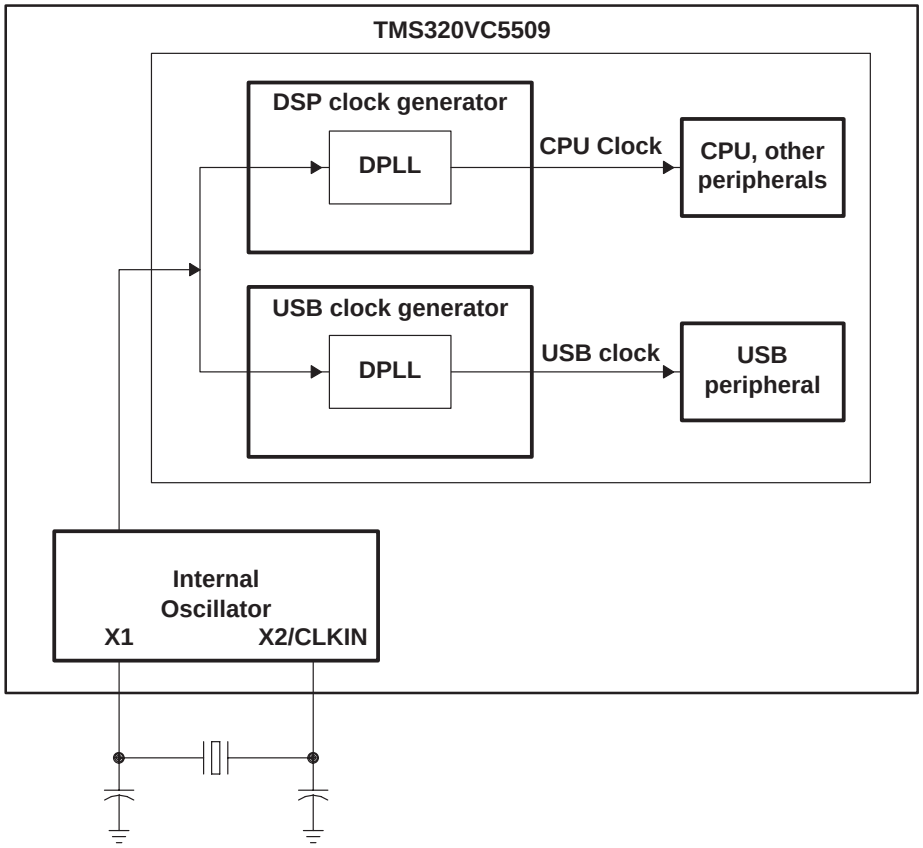

Figure 2. TMS320VC5509 USB Clock Generator

The TMS320VC5507 and TMS320VC5509A USB clock generators consist of an analog phase locked loop (APLL) as well as a DPLL. Figure 3 shows a diagram of the internal oscillator and its relationship to the clock generators.

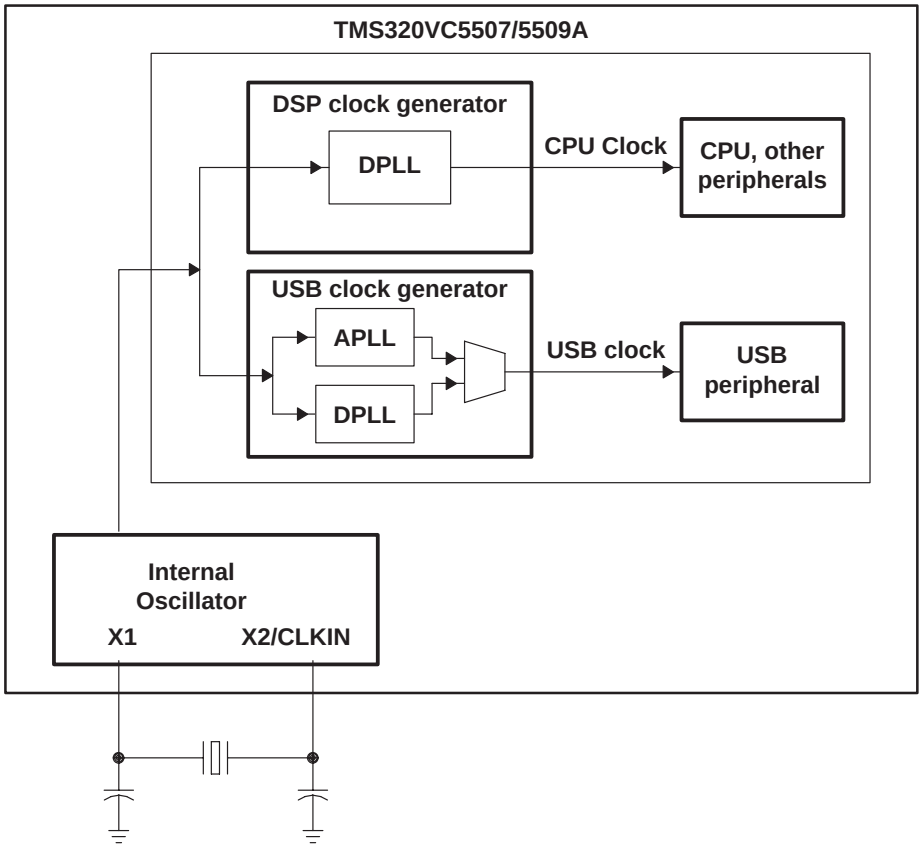

Figure 3. TMS320VC5507/5509A USB Clock Generator

Each clock generator also incorporates an IDLE mode for power conservation. It can be placed in its IDLE mode by turning off the CLKGEN IDLE domain in the IDLE configuration register (ICR). When the clock generator is idled, the output clock is stopped and held high. The IDLE status register (ISR) indicates which domains are currently idled, and the IDLE control register (ICR) indicates which domains will be active the next time the IDLE instruction is executed. Please note that the TMS320VC5507/5509A USB APLL is not part of the USB CLKGEN and cannot be IDLEd. In order to idle the USB PLL, the user has to switch to the USB DPLL from the APLL and then enter IDLE. See the *Using the USB APLL on the TMS320VC5507/5509A* applicaton report (SPRA997) for details on this procedure.

The DSP and USB clock generators are independent. If an IDLE instruction turns off the DSP clock generator, the USB module can keep running and vice versa. If either the DSP clock generator or the USB clock generator are idled using the IDLE power-down feature, the internal clock oscillator remains active. To disable the internal clock oscillator, both the DSP clock generator and the USB clock generator must be enabled before the IDLE power-down sequence can be initiated. This is also true for the case where a system does *not* incorporate a USB port or interface.

2 Disabling The Internal Oscillator

Figure 4 shows a complete block diagram and step-by-step details on how to disable the internal clock oscillator for the TMS320VC5509. Figure 5 shows the same procedure for the TMS320VC5507/5509A. Please note that if the on-chip emulation is used on the TMS320VC5507/5509A, the user must disconnect the emulator in order for the device to go into IDLE properly. If the emulator is left connected, the DSP will not go into IDLE.

Attached with this document is a sample assembly program that demonstrates the oscillator disable process for Figure 5.

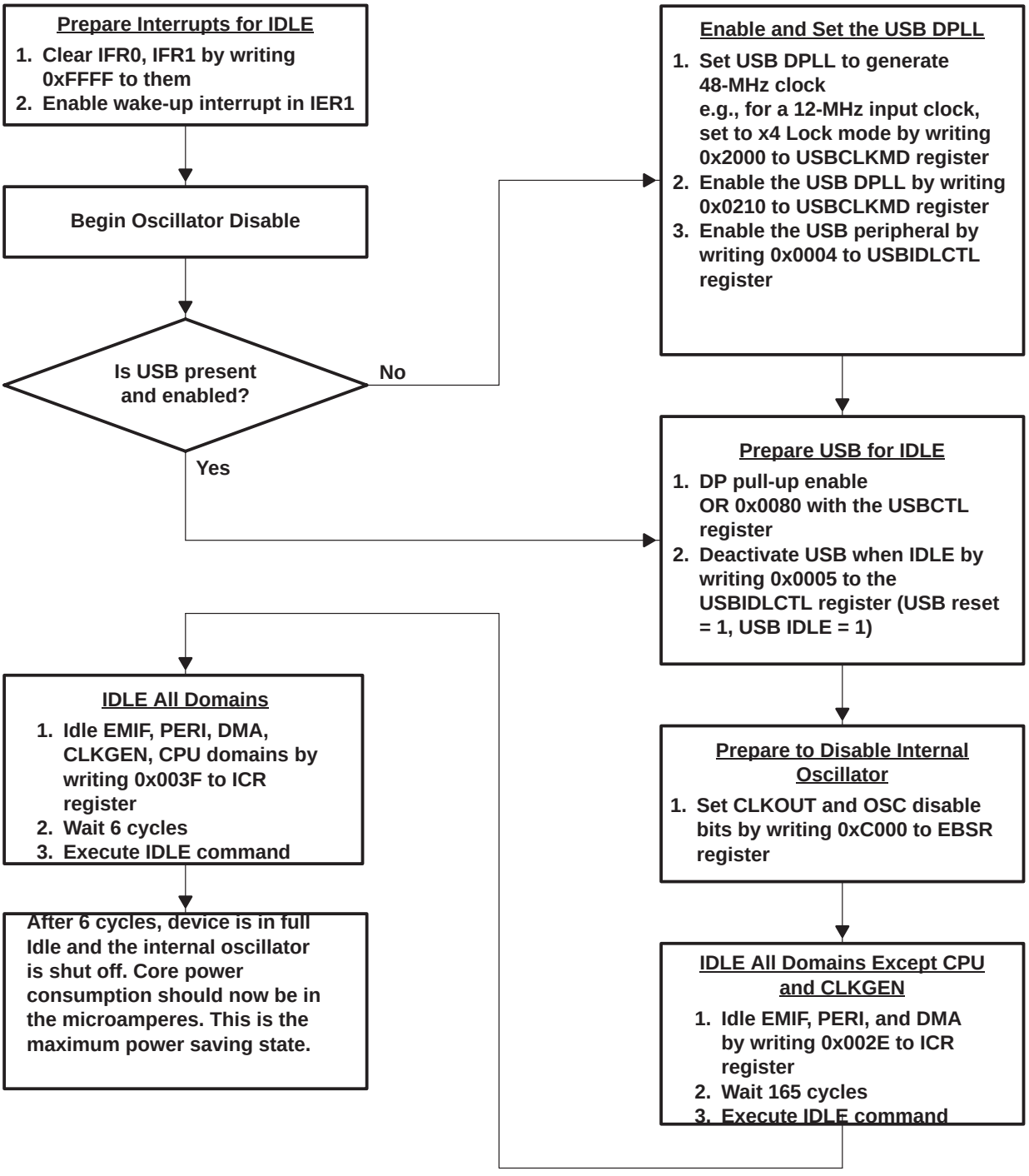

Figure 4. Disabling the Internal Oscillator on the TMS320VC5509

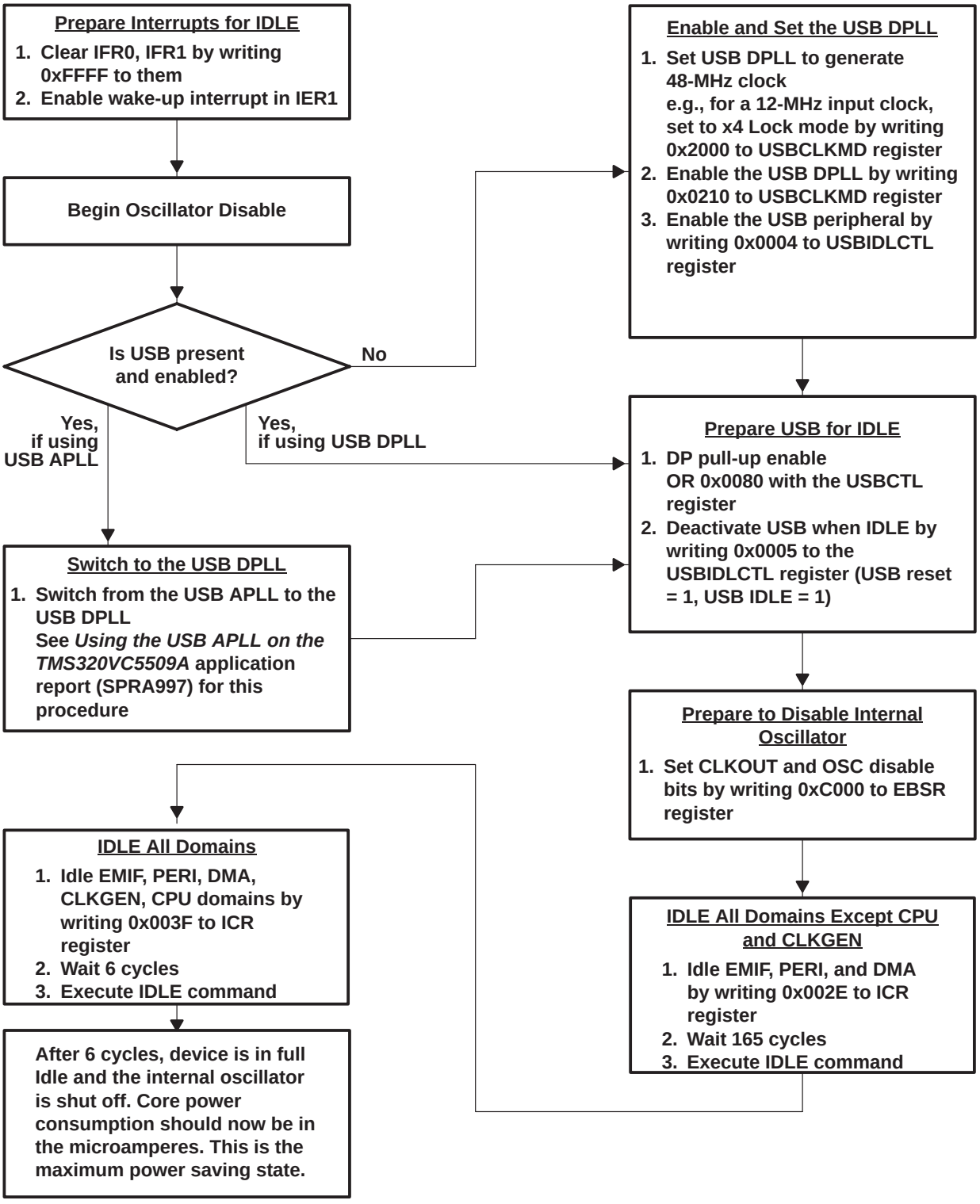

Figure 5. Disabling the Internal Oscillator on the TMS320VC5507/5509A

3 Enabling The Internal Oscillator

The internal oscillator can be awakened from IDLE mode with any of the four events shown below:

1. Hardware RESET
2. USB resume/reset events
3. Real-time clock (RTC) interrupt
4. External interrupt

Please note that all external interrupts are automatically masked when powering up from an IDLE state. This is needed because it gives the oscillator time to stabilize when being powered up. The TMS320VC5507, TMS320VC5509, and TMS320VC5509A use the USB DPLL as the time keeper, to allow time for this to happen. Therefore, if USB DPLL is not set up correctly, external interrupts will not be re-activated after wake up.

After wake up, the INTM bit in the status register ST1, and the respective IER register bits for the various interrupts, should be set to enable the CPU to execute interrupt service routines.

Also, note that after wakeup only the CLKGEN and CPU domains are awakened. It is the user's responsibility to enable the other domains by clearing the IDLEEN bit and setting the ICR appropriately. Afterwards, the user must use the IDLE command to execute these changes. The IDLE command is not pipeline protected, so extra cycles are required between the ICR assignment and the IDLE command (6 cycles are recommended). For more details on pipeline protection and operation, refer to *TMS320C55x DSP Programmer's Guide* (SPRU376).

Any wake-up event must consider the oscillator stabilize time. Since typically, most oscillators take at least 100–200 ms to stabilize, any wake-up event must typically be asserted for 10 CPU clock cycles + oscillator stabilize time. Oscillator stabilize time can be obtained for the specific manufacturer's oscillator being used.

For each system, the user must evaluate the oscillator stabilization time. This is an analog parameter that is affected by the board parasitics, crystal characteristics, temperature, and I/O supply voltage. Also, the ESR and the Load Capacitance (including parasitic capacitance) of the oscillator circuit influence the oscillator stability time. Lower DVdd voltages require longer oscillator stabilization times, and lower CVdd require longer PLL lock times.

You must wait for 1ms after the PLL lock bit is set before the PLL wrapper has locked onto the PLL clock and switches from the bypass clock to the new PLL clock. After the PLL lock bit is set, the PLL core has locked onto the oscillator clock, and will being outputting the PLL clock to the PLL wrapper. If you do not wait for the PLL wrapper to output the PLL clock to the rest of the chip, the CPU could potentially latch up if it is still running in bypass mode and trying to interface with faster devices.

Figure 6 and Figure 7 show each of the wake up procedures for TMS320VC5509 in detail.

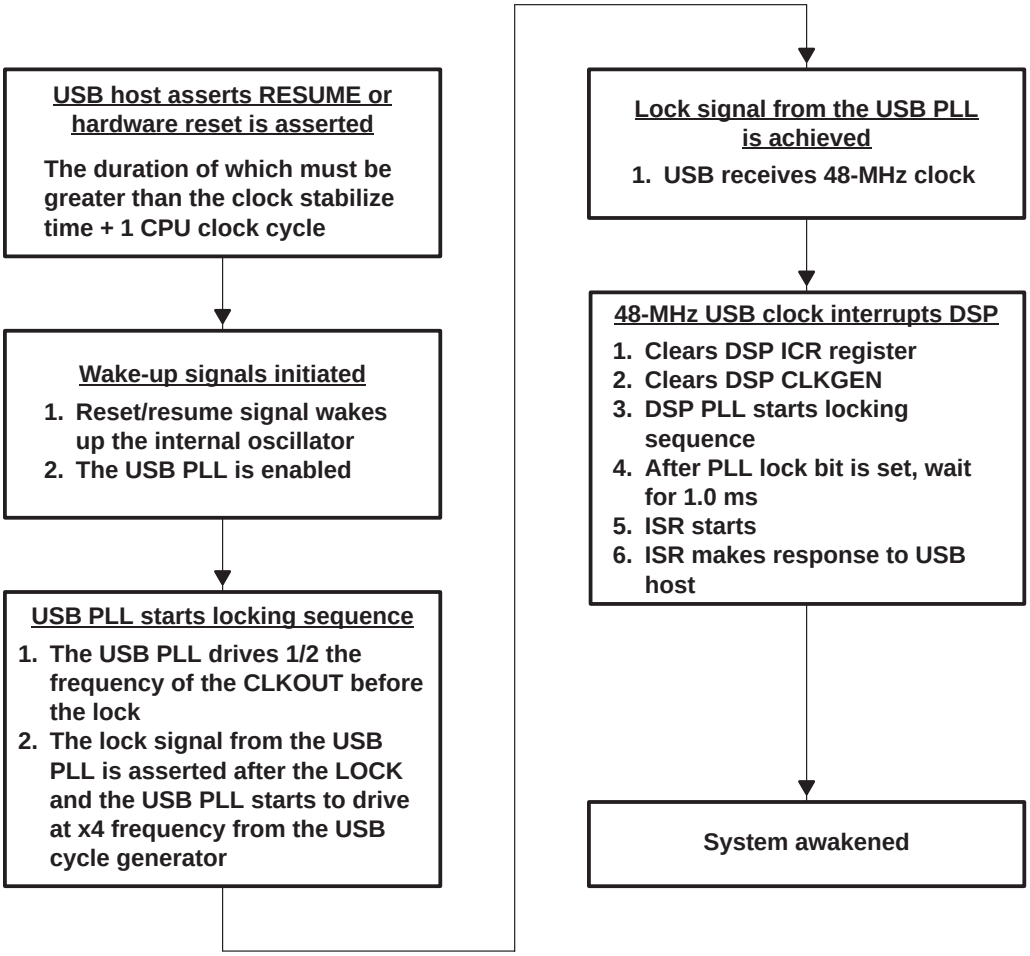

Figure 6. Waking Up the Internal Oscillator With a Hardware or USB Reset/Resume for the TMS320VC5509

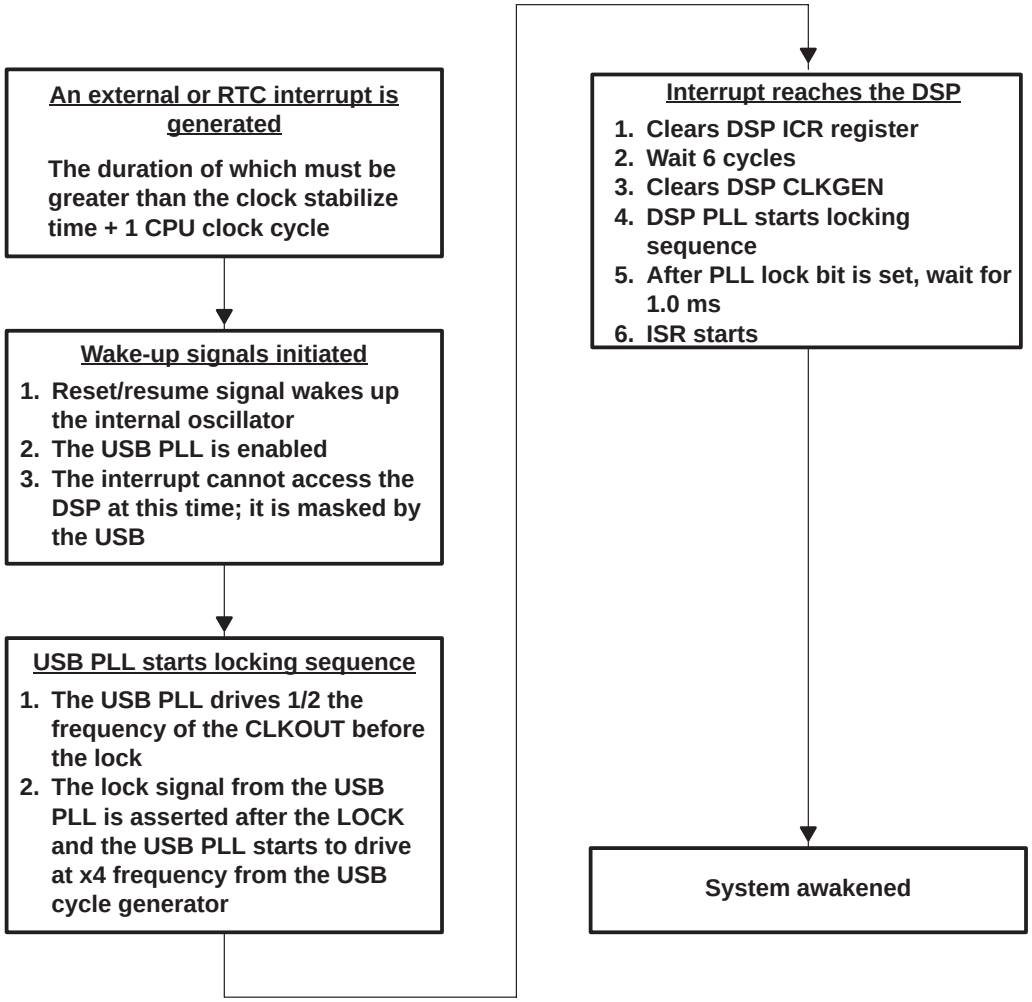

Figure 7. Waking Up the Internal Oscillator With an RTC or External Interrupt for the TMS320VC5509

Figure 8 and Figure 9 show each of the wake up procedures for TMS320VC5507/5509A in detail.

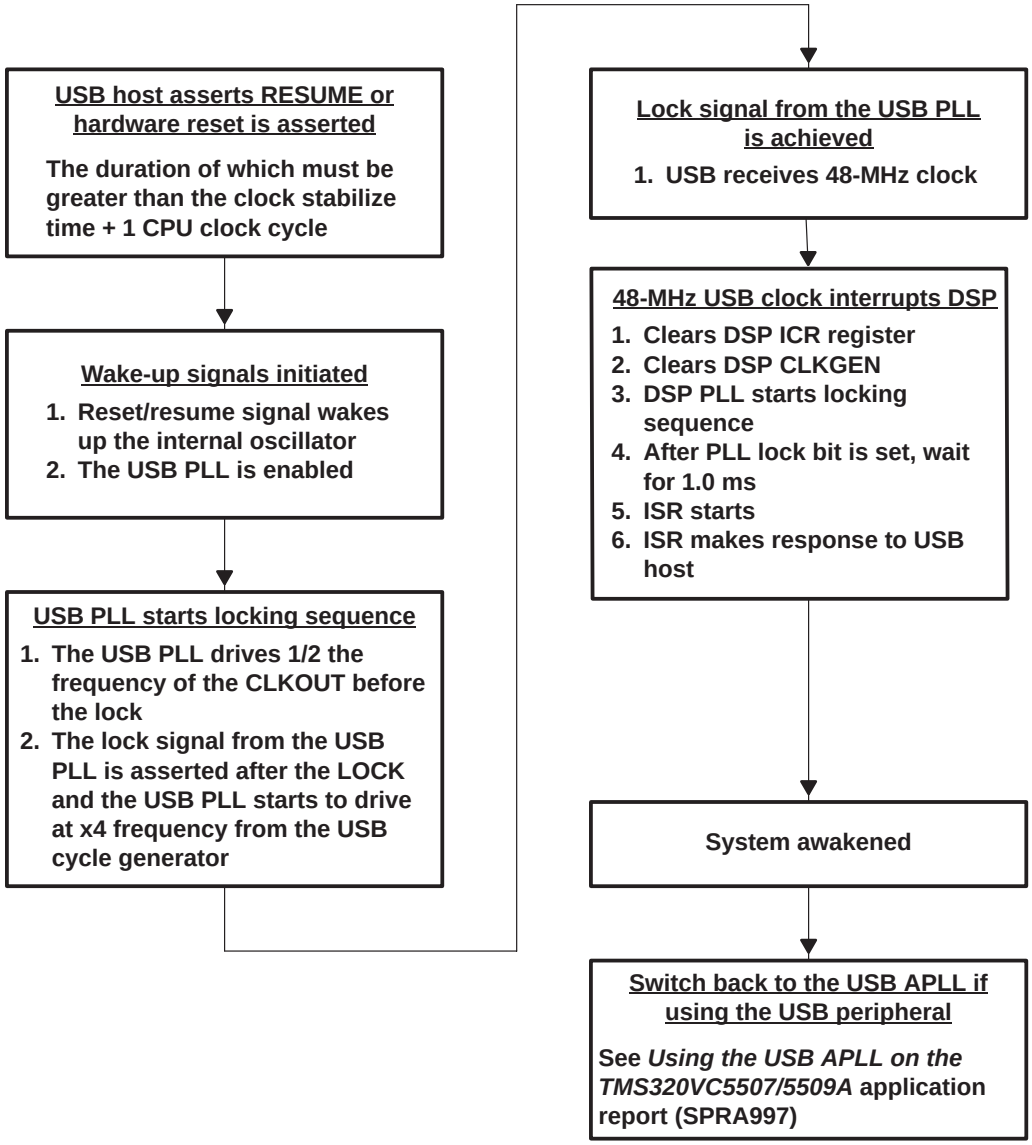

Figure 8. Waking Up the Internal Oscillator With a Hardware or USB Reset/Resume for the TMS320VC5507/5509A

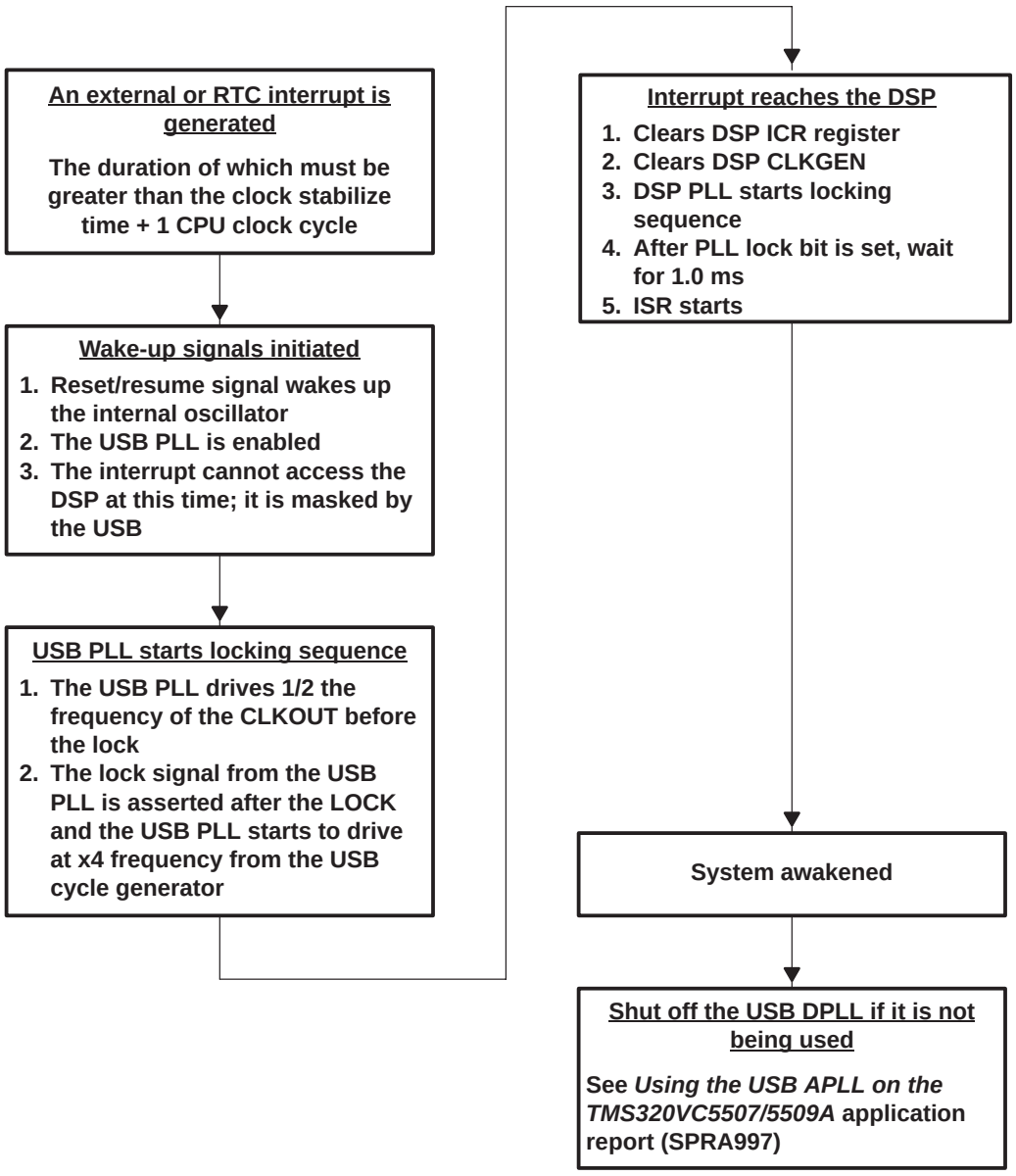

Figure 9. Waking Up the Internal Oscillator With an RTC or External Interrupt for the TMS320VC5507/5509A

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